Since the gate threshold voltage is determined by the sheet impurity concentrations of the barrier layer **64** and p-type channel layer **102**, the p-type channel layer may be formed only in the vicinity of the hetero interface.

FIG. **27** is a sectional view schematically showing a second modification of the HFET **310** shown in FIG. **25**. The characteristics of an HFET **314** shown in the drawing lie in that the p-type channel layer **102** is connected to a source electrode **104**. By this structure, since the hole generated at an avalanche breakdown is quickly discharged, the avalanche withstanding capability is increased. However, when the impurity concentration of the p-type channel layer **102** is excessively high in the structure shown in FIG. **27**, the channel layer is not depleted when the voltage is applied, the avalanche breakdown occurs at a low voltage, and there is a possibility that the breakdown voltage drops. To solve the problem, it is preferable to use the structure in which the p-type channel layer **102** is also depleted so as to obtain a high breakdown voltage when the voltage is applied to the layer. Specifically, the sheet impurity concentration of the p-type channel layer **102** is set to be substantially equal to that of the barrier layer **64**.

FIG. **28** is a sectional view schematically showing a third modification of the HFET **310** shown in FIG. **25**. In addition to the structure shown in FIG. **27**, an HFET **316** shown in FIG. **28** further comprises a field plate electrode **34** which is formed so as to cover the gate electrode **16** via the field insulating film **32** and which is connected to the source electrode **104**. By this structure, since the electric field in the end portion of the gate electrode **16** is defused, it is possible to increase the breakdown voltage of the device. Furthermore, even when the field plate electrode **36** is additionally disposed on the drain side on the field insulating film **32** as in an HFET **318** shown in FIG. **29**, it is possible to further increase the breakdown voltage.

ELEVENTH EMBODIMENT

FIG. **30** is a sectional view schematically showing a constitution of an eleventh embodiment of the semiconductor device according to the present invention. The characteristics of a MIS-HFET **320** shown in the drawing lie in that the transistor further comprises a gate insulating film **84** formed on the surface of the barrier layer **64** and that the gate electrode **16** is formed in a concave portion of the barrier layer **64** via the gate insulating film **84**. The present invention is also applicable to such MIS gate structure. Furthermore, when the field plate electrode **34** is disposed so as to cover the gate electrode **16** via the field insulating film **32** as in modifications **322** and **324** shown in FIGS. **31** and **32**, respectively, a field concentration in the end of the source electrode **12** or the drain electrode **14** is defused, and it is possible to further increase the breakdown voltage.

Furthermore, when the p-type channel layer **102** is connected to the source electrode **104** as in a MIS-HFET **326** shown in FIG. **33**, the hole can be quickly discharged, and it is therefore possible to increase the avalanche withstanding capability.

The first to eleventh embodiments of the present invention have been described above, but the present invention is not limited to the above-described embodiments, and any person skilled in the art can easily devise various other modifications within the scope of the present invention.

For example, the channel layer **2**, base layer **6**, and buffer layer **8** have been described using the GaN layer, but an AlGaN layer can be implemented, when an equal Al composition ratio is set to each of three layers, and set to be smaller than that of the barrier layer **4**. Moreover, with respect to the Al composition ratio of the buffer layer **8**, the channel layer **2** is equal to the base layer **6**, but different composition ratios may also be used. However, the Al composition ratio of the buffer layer **8** is preferably equal to that of the channel layer **2** in order to cancel the piezo polarization in the hetero interface between the barrier layer **4** and the channel layer **2** and to lower the 2DEG carrier concentration under the gate electrode.

Moreover, the invention can be implemented as long as a relation between band gaps is the same even when the band gaps are changed by a composition ratio such as a case where an InGaN layer is used for the channel layer and a GaN layer is used for the barrier layer and a case where an AlGaN layer is used for the channel layer and an AlN layer is used for the barrier layer.

Furthermore, an i-AlGaN layer may also be inserted between the channel layer **2** and the barrier layer **4** or between the barrier layer **4** and the base layer **6** in order to keep steepness of modulation doping or hetero interface.

Additionally, the semiconductor layers such as the channel layer and barrier layer may be formed by the crystal growth on the substrate, and may be implemented with substrates such as GaN, SiC, sapphire, and Si, but the present invention is not limited to the material of the substrate, and a buffer layer or the like involved by the crystal growth may also be formed under the channel layer.

Moreover, in the present invention, a threshold voltage can be shifted on a plus side even in a normally-on device by forming the GaN layer on the AlGaN barrier layer for the purpose of realizing the normally-off state. Especially, the Al composition ratio of the base layer **6** is equal to that of the channel layer **2**. However, in a meaning that the carrier by the piezo polarization is reduced, even when the Al composition ratio is not equal, the present invention may be implemented with an Al composition ratio smaller than that of the barrier layer **4**.

What is claimed is:

1. A semiconductor device, comprising:

a first semiconductor layer represented by a composition formula $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$);

a first conductivity type or non-doped second semiconductor layer represented by a composition formula $Al_yGa_{1-y}N$ ($0 \leqq y \leqq 1, x<y$) and is formed on the first semiconductor layer;

a second conductivity type third semiconductor layer represented by a composition formula $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) and is selectively formed above the second semiconductor layer;

a gate insulator formed on the third semiconductor layer;

a gate electrode formed on the gate insulator;

a source electrode electrically connected to the second semiconductor layer;

a drain electrode electrically connected to the second semiconductor layer; and

a fourth semiconductor layer represented by a composition formula $Al_zGa_{1-z}N$ ($1 \leqq z \leqq 1$) and is formed so as to be inserted between the second semiconductor layer and the third semiconductor layer.

2. The semiconductor device according to claim **1**,

wherein the sheet impurity concentration of the third semiconductor layer is equal to or more than the sheet impurity concentration of the second semiconductor layer.

3. A semiconductor device, comprising:

a first semiconductor layer represented by a composition formula $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$);